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CPEG 324

LAB 1

3/3/17

**ISA Simulator Implementation:**

* My simulator had an overall similar design with my partner’s. The simulator takes in a text file with binary inputs line by line, reads/separates bits according to opcodes, source and result registers and computes instructions based on the opcodes present in each line
* I added additional test cases for the benchmark, testing the skip functions in both of our source codes, I also tested the addition of blank lines in the test cases and this did not affect functionality of the program.
* I included a check for file red error/success to prevent reading files with incorrect binary format
* Running tests on my team-mates simulator did not result in program termination or lag. The ISA was able to perform key operations outlined in the project description.